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10/810,618	03/29/2004	Toshiaki Inoue	04151-5391	9830

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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,618	INOUE, TOSHIAKI	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/29/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

2. Acknowledgment is made of applicant's claim for priority under 35 U.S.C. 119(a)-(d) based upon an application filed in Japan on March 28, 2003.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on March 29, 2004 was filed after the mailing date of the application on March 29, 2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Keith (US004785349A).

Keith describes a digital image processing device (*a system for compressing and formatting a full motion color digital video signal*, Col. 1, lines 42-43) comprising a signal processing unit (220, 230, Figure 2) to process a video input signal (S2; *processor 220 provides conversion of video signal S2*, Col. 6, lines 19-30); a frame memory (232) to store a result from the processing performed by the signal processing unit (*stores the complete sub-frames in a buffer store 232*, Col. 9, lines 15-22); and a redundant pixel embedding circuit (250) to embed a redundant pixel not to be displayed (*formatter 250 adds "padding" data*, Col. 6, lines 60-65) in image data read from the frame memory (S10, Figures 2 and 13; Col. 34, lines 53-56; *data read from the disk store 1350...switch 1390 inserts padding on data to individual frames of the sequence*, Col. 35, line 64-Col. 36, line 7) and to produce a video output signal (S4; Col. 37, lines 16-18). Keith describes that the image frame data is divided into groups of lines (*division of the compressed data into groups of lines*, Col. 1, lines 32-40; *512 pixels per active line interval*, Col. 8, line 31; *60 lines/picture height*, Col. 8, lines 45-51), and therefore the image data read from the frame memory is inherently an image line.

Thus, it reasonably appears that Keith describes or discloses every element of the claim and therefore anticipates the claim subject.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 2, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keith (US004785349A) in view of O'Sullivan (US005896140A).

9. With regard to Claim 2, Keith describes a redundant pixel embedding circuit (250) to embed a redundant pixel not to be displayed (*formatter 250 adds "padding" data*, Col. 6, lines 60-65) in image data read from the frame memory (S10, Figures 2 and 13; Col. 34, lines 53-56; *data read from the disk store 1350...switch 1390 inserts padding on data to individual frames of the sequence*, Col. 35, line 64-Col. 36, line 7). Keith describes that the image frame data is divided into groups of lines (*division of the compressed data into groups of lines*, Col. 1, lines

32-40; *512 pixels per active line interval*, Col. 8, line 31; *60 lines/picture height*, Col. 8, lines 45-51), and therefore the image data read from the frame memory is inherently an image line.

However, Keith does not specifically teach that the redundant pixel embedding circuit has a function of embedding, according to an embedding control signal fed from outside, a redundant pixel in a specified position in the image line. However, O'Sullivan describes that the redundant pixel embedding circuit (44, Figure 2) has a function of receiving, as an input, an image line (Col. 12, line 65-Col. 13, line 1) read from the signal processing unit (42; Col. 7, lines 17-24) and of embedding, according to an embedding control signal fed from outside (*frame grabber controller 52 provides the dummy pixel value to the dummy pixel logic 53, which controls the clocking in of data from the decoder/scaler 44 to provide the proper number of dummy video pixels before each horizontal scan line of video pixels*, Col. 15, lines 20-26), a redundant pixel in a specified position in the image data (Col. 14, line 56-Col. 15, line 6).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Keith so that the redundant pixel embedding circuit has a function of embedding, according to an embedding control signal fed from outside, a redundant pixel in a specified position in the image line as suggested by O'Sullivan because O'Sullivan suggests that this is needed in order to prevent losing video pixels and/or restrict the placement of a video window on the computer screen (Col. 2, lines 62-65; Col. 14, line 33-67).

10. With regard to Claim 8, Claim 8 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

11. With regard to Claim 9, Claim 9 is similar in scope to Claim 2, and therefore is rejected under the same rationale.

12. Claims 3, 4, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keith (US004785349A) in view of Mori (US005060059A).

13. With regard to Claim 3, Keith describes a digital image processing device (*a system for compressing and formatting a full motion color digital video signal*, Col. 1, lines 42-43) comprising a signal processing unit (220, 230, Figure 2) to process a video input signal (S2; *processor 220 provides conversion of video signal S2*, Col. 6, lines 19-30); a frame memory (232) to store a result from the processing performed by the signal processing unit (*stores the complete sub-frames in a buffer store 232*, Col. 9, lines 15-22); and a redundant pixel embedding circuit (250) to embed a redundant pixel not to be displayed (*formatter 250 adds "padding" data*, Col. 6, lines 60-65) in image data read from the frame memory (S10, Figures 2 and 13; Col. 34, lines 53-56; *data read from the disk store 1350...switch 1390 inserts padding on data to individual frames of the sequence*, Col. 35, line 64-Col. 36, line 7) and to produce a video output signal (S4; Col. 37, lines 16-18). Keith describes that the image frame data is divided into groups of lines (*division of the compressed data into groups of lines*, Col. 1, lines 32-40; *512 pixels per active line interval*, Col. 8, line 31; *60 lines/picture height*, Col. 8, lines 45-51), and therefore the image data read from the frame memory is inherently an image line.

However, Keith does not teach that the device includes a serial-parallel converting circuit and a parallel-serial converting circuit. However, Mori describes a digital image processing

device comprising a signal processing unit (110, Figure 6) to process a video input signal (100; Col. 5, lines 19-25); a serial-parallel converting circuit (201) to receive image data read from signal processing unit (Col. 5, lines 24-39). Mori describes that the image data from the signal processing unit is color-sequential color image data, and it is supplied to a time base conversion unit 200a which converts the frequency of the image data (Col. 5, lines 24-34). Since the data is sequential and has a frequency, the serial-parallel converting circuit receives the data in a time-series manner (Col. 5, lines 30-39) and produces an output (Col. 5, lines 36-39). The output from the serial-parallel converting circuit is input into a line buffer (207), as can be seen in Figure 6, and therefore the serial-parallel converting circuit produces an output making up an image line. Mori describes that the output from the serial-parallel converting circuit (201, Figure 6; 10, Figure 1) is input into the adder (17; Col. 4, lines 9-42), and the adder receives dummy data (Col. 4, lines 49-52). The output of the adder is input into a parallel-serial converting circuit (241, Figure 14; 211, Figure 6; 5, Figure 1;.Col. 4, lines 49-56; Col. 9, lines 49-55), which outputs the image line in which the dummy data is embedded as color-sequential image data or time-series image data (Col. 9, lines 50-65).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Keith so that the device includes a serial-parallel converting circuit and a parallel-serial converting circuit as suggested by Mori because Mori suggests that data converters for conversion of color-sequential image data into parallel data in the masking circuit and in the black extraction circuit where parallel image data are needed, and effects image processing on color-sequential image data in other sections have the advantages of reducing the

number of circuit components and compactizing the apparatus; and reducing the cost of the color image processing apparatus (Col. 5, lines 4-15).

14. With regard to Claim 4, Keith describes a redundant pixel embedding circuit (250) to embed a redundant pixel not to be displayed (*formatter 250 adds "padding" data*, Col. 6, lines 60-65) in image data read from the frame memory (S10, Figures 2 and 13; Col. 34, lines 53-56; *data read from the disk store 1350...switch 1390 inserts padding on data to individual frames of the sequence*, Col. 35, line 64-Col. 36, line 7). Keith describes that the image frame data is divided into groups of lines (*division of the compressed data into groups of lines*, Col. 1, lines 32-40; *512 pixels per active line interval*, Col. 8, line 31; *60 lines/picture height*, Col. 8, lines 45-51), and therefore the image data read from the frame memory is inherently an image line.

However, Keith does not teach a serial-parallel converting circuit which is made up of a register file being able to store an image line and which has a function of sequentially storing image data fed from the frame memory in a time-series manner according to a writing control signal fed from outside and of reading, simultaneously and in parallel, contents of all registers in the register file. However, Mori describes that the serial-parallel converting circuit (201, Figure 6; 10, Figure 1) which is made up of a register file (40-44, Figure 5) being able to store an image line and which has a function of sequentially storing image data (7) fed from the signal processing unit (110, Figure 6; 1, Figure 1; Col. 3, lines 38-45) according to a writing control signal (46, Figure 5) fed from outside (45; *latch controller 45 for releasing latch signals 46 for the registers in response to the mode signal 6 and the clock signal 8*, Col. 4, line 58-Col. 5, line 3). Since the latch signal is controlled by the clock signal, the image data is fed in a time-series

manner. Mori describes that the serial-parallel converting circuit reads, simultaneously and in parallel, contents of all registers in the register file (*data converter releases 8-bit color image data in parallel manner*, Col. 5, lines 2-3). This would be obvious for the same reasons give in the rejection for Claim 3.

15. With regard to Claim 10, Claim 10 is similar in scope to Claim 3, and therefore is rejected under the same rationale.

16. With regard to Claim 11, Claim 11 is similar in scope to Claim 4, and therefore is rejected under the same rationale.

17. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keith (US004785349A) in view of Mori (US005060059A), further in view of O'Sullivan (US005896140A).

18. With regard to Claim 5, Keith and Mori are relied upon for the teachings as discussed above relative to Claim 3. Keith describes a redundant pixel embedding circuit (250, *formatter 250 adds "padding" data*, Col. 6, lines 60-65).

However, Keith does not teach that the redundant pixel embedding circuit has a function of receiving, as an input, the image line read from the serial-parallel converting circuit. However, Mori describes that the adder (17, Figure 1; 210, Figure 6), which receives dummy data (Col. 4, lines 49-56), receives data from the data converter (10), as can be seen in Figure 1.

The adder is equivalent to the selector 210 of Figure 6 (Col. 6, lines 62-67), and the data converter (10; *data is supplied to a data converter 10 for conversion into 6-bit parallel image data*, Col. 3, lines 45-49) is equivalent to the serial-parallel converting circuit 201 of Figure 6 (Col. 5, lines 34-39). The output from the serial-parallel converting circuit is input into a line buffer (207), and the output from the line buffer is input into the selector, as can be seen in Figure 6. Therefore, the adder has a function of receiving, as an input, the image line read from the serial-parallel converting circuit (10, Figure 1; 201, 207, Figure 6). This would be obvious for the same reasons given in the rejection for Claim 3.

However, Keith and Mori do not specifically teach embedding, according to an embedding control signal fed from outside, a redundant pixel in a specified position in the image line. However, O'Sullivan describes that the redundant pixel embedding circuit (44, Figure 2) has a function of receiving, as an input, an image line (Col. 12, line 65-Col. 13, line 1) read from the signal processing unit (42; Col. 7, lines 17-24) and of embedding, according to an embedding control signal fed from outside (*frame grabber controller 52 provides the dummy pixel value to the dummy pixel logic 53, which controls the clocking in of data from the decoder/scaler 44 to provide the proper number of dummy video pixels before each horizontal scan line of video pixels*, Col. 15, lines 20-26), a redundant pixel in a specified position in the image data (Col. 14, line 56-Col. 15, line 6), as discussed in the rejection for Claim 2.

19. With regard to Claim 12, Claim 12 is similar in scope to Claim 5, and therefore is rejected under the same rationale.

20. Claims 6, 7, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keith (US004785349A) in view of Mori (US005060059A), further in view of Hayashi (US005305122A), further in view of Heilveil (US004639890A).

21. With regard to Claim 6, Keith and Mori are relied upon for the teachings as discussed above relative to Claim 3.

However, Keith and Mori do not specifically teach that the parallel-serial converting circuit has a register file made up of shift registers. However, Hayashi describes that the parallel-serial converting circuit (7, Figure 3) has a register file made up a shift register (*shift register 7 is a 16-bit parallel-serial converte*r, Col. 9, lines 25-29) and a selector (9) to select an output from the shift register and to output the selected output (*selector 9 selects either the output from the shift register 7 or a signal at ground voltage "0" as an output VD*, Col. 7, lines 1-3) and wherein the register file is able to store an image line in one clock cycle (Col. 13, lines 45-47) and wherein the shift register is able to perform a shifting operation, according to a reading control signal fed from outside, in synchronization with a clock signal (20; Col. 7, lines 4-10) and wherein the selector (31, Figure 9) has a function of selecting a specified shift output from the shift register and of outputting the selected output according to an embedding control signal fed from outside (32; Col. 8, lines 31-35).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Keith and Mori so that the parallel-serial converting circuit has a register file made up of a shift register as suggested by Hayashi. It is well-known in the art

that parallel-serial converting circuits are shift registers. This can be found in many publications, such as Bigelow's website.

However, Keith, Mori, and Hayashi do not teach that the register file is made up of two or more shift registers. However, Heilveil describes that the parallel-serial converting circuit (a serial shift register for interconnection in parallel with the columns of cells, Col. 2, lines 46-48) has a register file (20, Figure 3) made up of two or more shift registers (*shift register 20 split into two identical halves*, Col. 6, lines 18-22) and a selector (26, Figure 2) to select an output from each of the shift registers and to output the selected output (Col. 6, lines 34-37) and wherein each of the shift registers is able to perform a shifting operation, according to a reading control signal fed from outside, in synchronization with a clock signal (*shift register 20 is operated by a clock which is used to shift the bits through the stages of the register*, Col. 6, lines 38-46).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Keith, Mori, and Hayashi so that the register file is made up of two or more shift registers as suggested by Heilveil because Heilveil suggests that splitting the shift register in half and placing the halves on opposite sides of the array balances the operation of the sense amplifiers (Col. 6, lines 16-26).

22. With regard to Claim 7, Keith, Mori, and Hayashi do not teach split shift registers. However, Heilveil describes that each of the shift registers (20, Figure 3) is made up of two or more split shift registers (*shift register 20 split into two identical halves*, Col. 6, lines 16-26) and wherein each of the split shift registers receives a data input (Col. 6, lines 32-37), shift data input (Col. 6, lines 38-40), latch signal input (Col. 4, lines 46-56), and shift signal input (Col. 6, lines

42-46) and produces a shift data output (Col. 6, lines 32-37) and wherein each of the shift registers has a function of writing, when data is to be written to the split shift registers, data at one time, by making active a latch signal input, in synchronization with a clock (Col. 6, lines 47-65) and, at time of shifting operations, of performing the shifting operation for data, by making active a shift signal input, in synchronization with a clock (Col. 6, lines 42-46) and of feeding a shift output fed from each of the split shift registers to the selector (26, Figure 2) by connecting a terminal for a shift output from each of the split shift registers to allow the shift register to perform the shift operation as a whole (Col. 6, lines 34-37). This would be obvious for the same reasons give in the rejection for Claim 6.

23. With regard to Claim 13, Claim 13 is similar in scope to Claim 6, and therefore is rejected under the same rationale.

24. With regard to Claim 14, Claim 14 is similar in scope to Claim 7, and therefore is rejected under the same rationale.

Prior Art of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Kimura (US 20020130974A1) teaches a signal processing unit (5, Figure 2) to process a video input signal (3, [0030], lines 5-6), and writing dummy data (9) onto a line memory within the signal processing data path as redundant bits ([0016], lines 17-22).

2. Yun (US 20030197672A1) teaches a signal processing unit (141, Figure 14) [0132], a redundant pixel embedding circuit (dummy data generator) to embed a dummy data in an image line, and storing the dummy data [0035].

3. Bigelow, Ken. "Parallel-to-Serial Shift Register." http://www.play-hookey.com/digital/shift-out_register.html.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

U Chauhan

ULKA J. CHAUHAN
PRIMARY EXAMINER